coreboot - Bug #77

Skylake FPS1.1 without vboot has no CAR ramstage

10/06/2016 02:10 AM - Trammell Hudson

Status:	Resolved	**Start date:**	10/06/2016
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:	board support	**Estimated time:**	0.00 hour
Target version:			

Description

As discussed on the mailing list: https://www.coreboot.org/pipermail/coreboot/2016-October/082117.html

Building from git for Skylake with FPS 1.1 (the Chell Chromebook) without vboot enabled produces a coreboot image that hangs when it jumps into the romstage. The reason is that there is no car_stage_entry function, only a weak symbol with an infinite loop in src/arch/x86/assembly_entry.S.

Aaron Durbin hypothesized that the transition to Skylake using C_ENVIRONMENT_BOOTBLOCK might have broken this combination and suggested this patch:

```
diff --git a/src/drivers/intel/fsp1_1/Makefile.inc b/src/drivers/intel/fsp1_1/Makefile.inc
index 4ea23f3..025b067 100644
--- a/src/drivers/intel/fsp1_1/Makefile.inc
+++ b/src/drivers/intel/fsp1_1/Makefile.inc
@@ -28,7 +28,7 @@ romstage-y += fsp_util.c
 romstage-y += hob.c
 romstage-y += raminit.c
 romstage-y += romstage.c
-romstage-$(CONFIG_SEPARATE_VERSTAGE) += romstage_after_verstage.S
+romstage-y += romstage_after_verstage.S
 romstage-y += stack.c
 romstage-y += stage_cache.c
```

This works and allowed it to make further progress until rebooting in the ramstage (reported as a separate bug)

History

#1 - 05/13/2017 09:31 PM - Nico Huber

- Status changed from New to Resolved

Looks like this has been fixed by Teo Boon Tiong with

d8e34b2c44 driver/intel/fsp1_1: Fix boot failure for non-verstage case