coreboot - Feature #115

Consolidate Intel ICH7..PCH9 PIRQ configuration

05/10/2017 09:39 PM - Nico Huber

Status:	New	**Start date:**	05/10/2017
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:			

Description

There was already work going on to consolidate this. The idea was to set all PIRQs to IRQ 11 on the PICs. But this doesn't work in case one of the PIRQs is used in exclusive mode for an edge triggered interrupt.

So the whole IRQ routing has to be configurable. But we can provide sane defaults. We can use the default configuration for DxxIP/DxxIR registers in most cases and IRQ 11 for every PIRQ that isn't set in the devicetree but used through DxxIR or the northbridge (usually PINA only, always PIRQA???). All PIRQs used for PCI should be set to IRQ 11 to keep the configuration of the PCI_INTERRUPT_LINE registers simple (it's currently broken for all cases where we don't have the same IRQ for all PCI PIRQs, missing the configuration of internal devices and interrupt swizzling).

PIRQs that are used for edge triggered interrupts should be configured in the devicetree (replacing current pirq*_routing settings with an array!) and chipset code should configure the PICs (i8259_configure_irq_trigger()?).

History

#1 - 05/11/2017 12:00 PM - Nico Huber

It doesn't have to be fully configurable: A static configuration with PIRQA..PIRQD for integrated PCI devices should work for all boards.

#2 - 05/31/2018 09:49 AM - Arthur Heymans

Is implemented. Just has to be hooked up: https://review.coreboot.org/#/c/coreboot/+/22981/ and https://review.coreboot.org/#/c/coreboot/+/22980/